

# **Lindbergh Schematic Document**

## **uFCPGA Northwood**

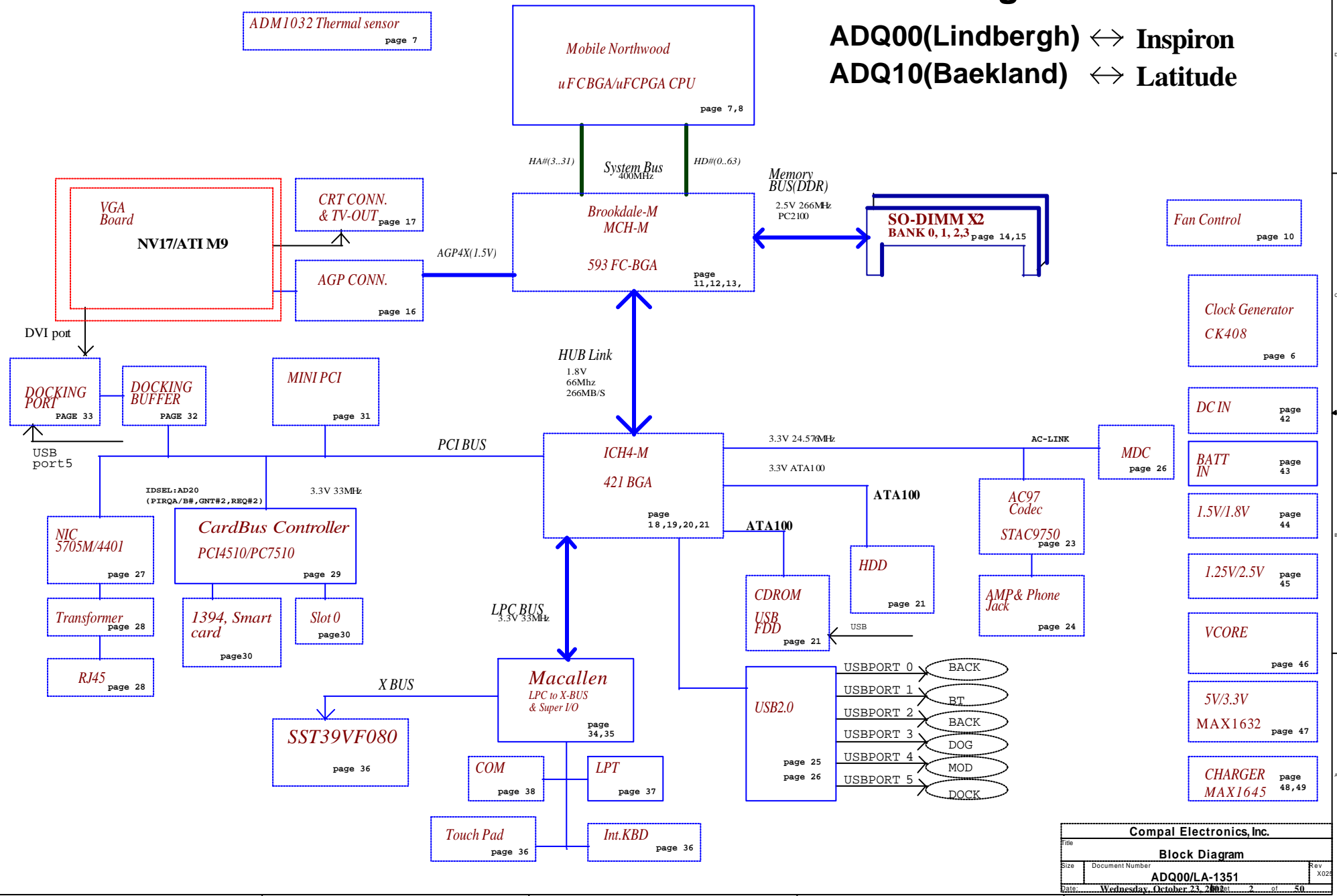
**2002-10-23**

**Rev:X025**

<b>Compal Electronics, Inc.</b>		
Title		
<b>Cover Sheet</b>		
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	<b>ADQ00/LA-1351</b>	<b>X025</b>
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# Block Diagram

ADQ00(Lindbergh) ↔ Inspiron  
ADQ10(Baekland) ↔ Latitude



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Block Diagram			
ADQ00/LA-1351			
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## D

C

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8

## A

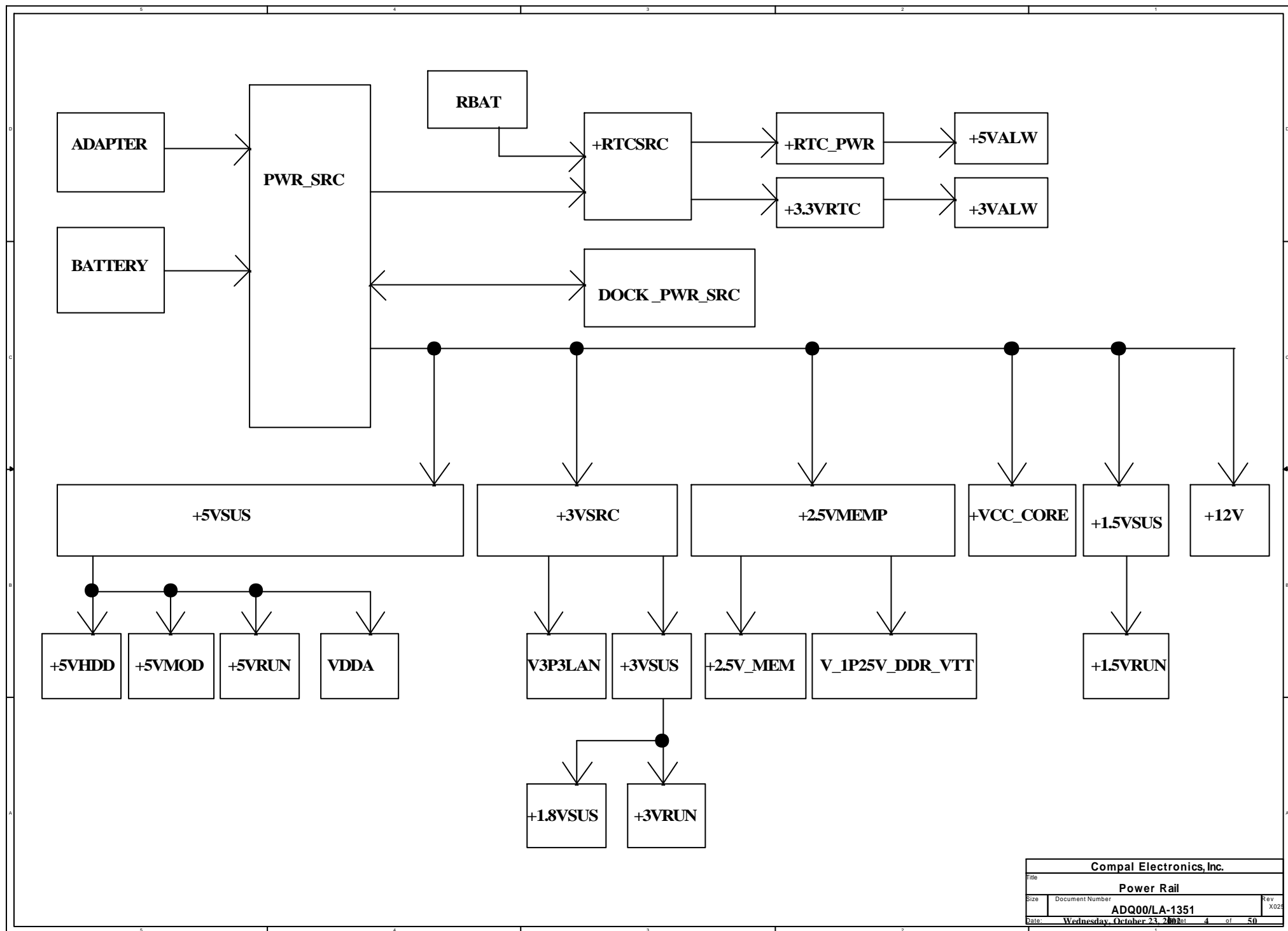
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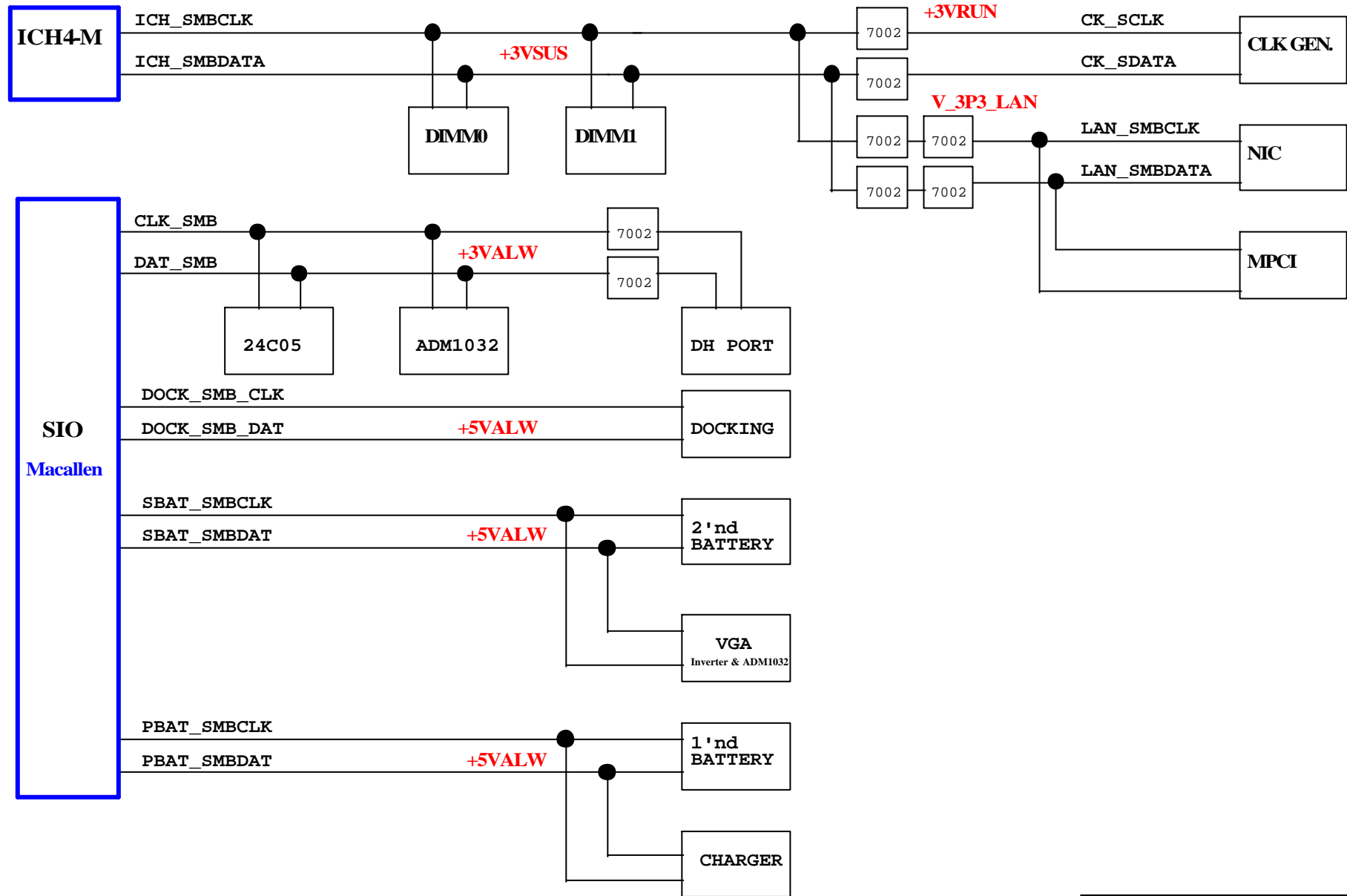
**Baekland- 43122231001, with 1@**

**Note:** "@" means all model depop  
 "?" means Kapalua pop only (ie Lendbergh depop)  
 "#" means Lindbergh pop only (ie baekland depop)

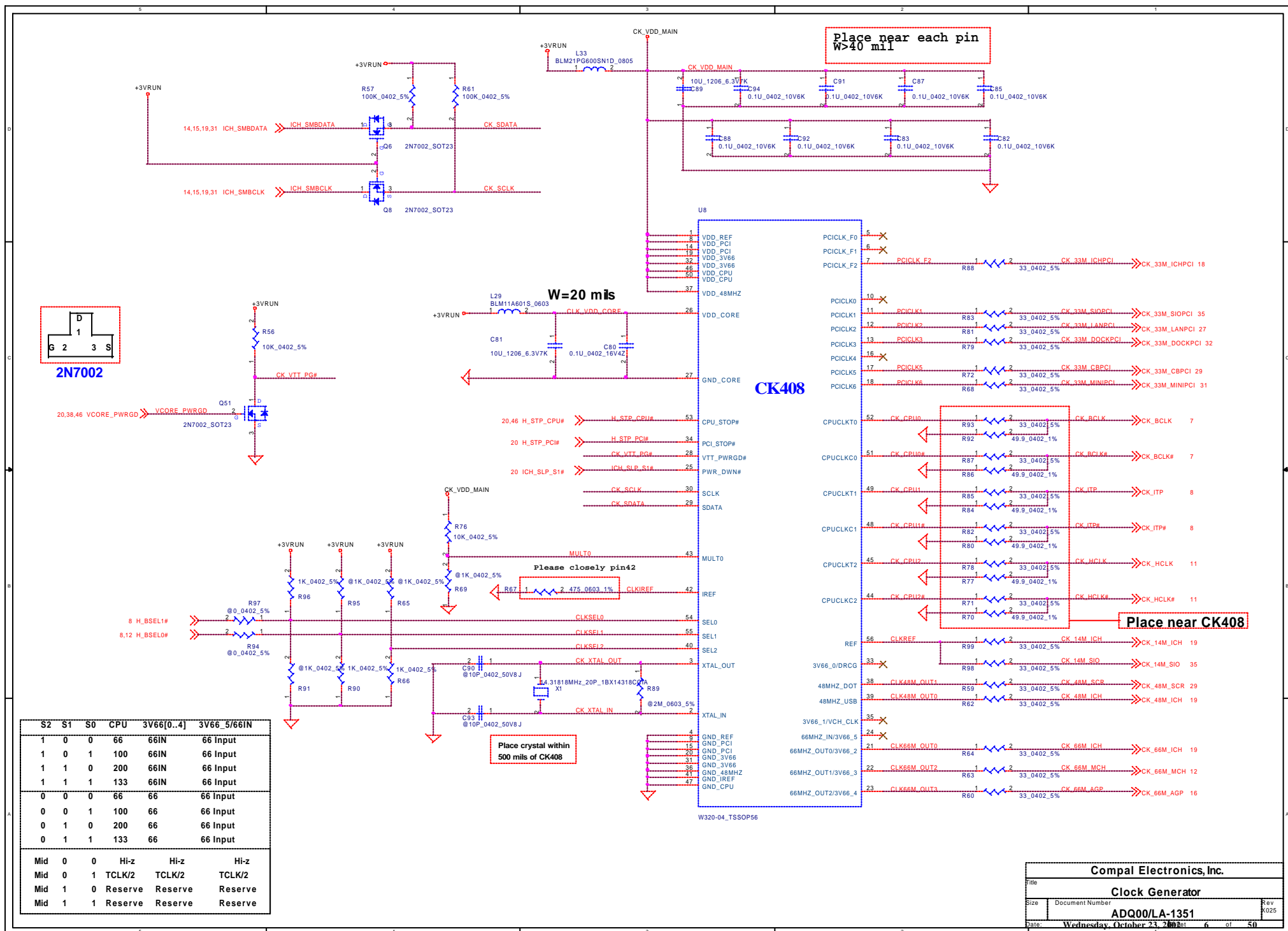
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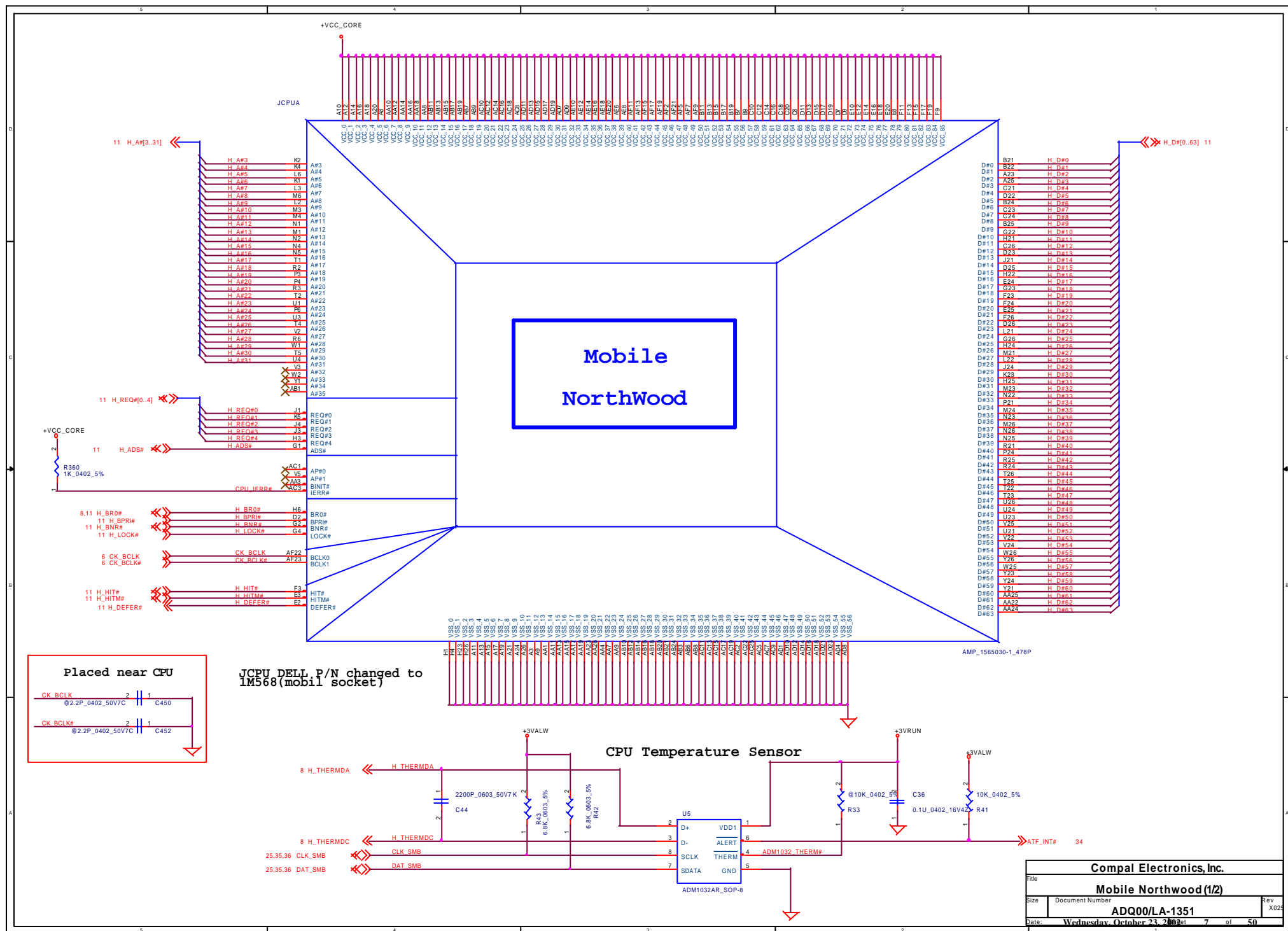
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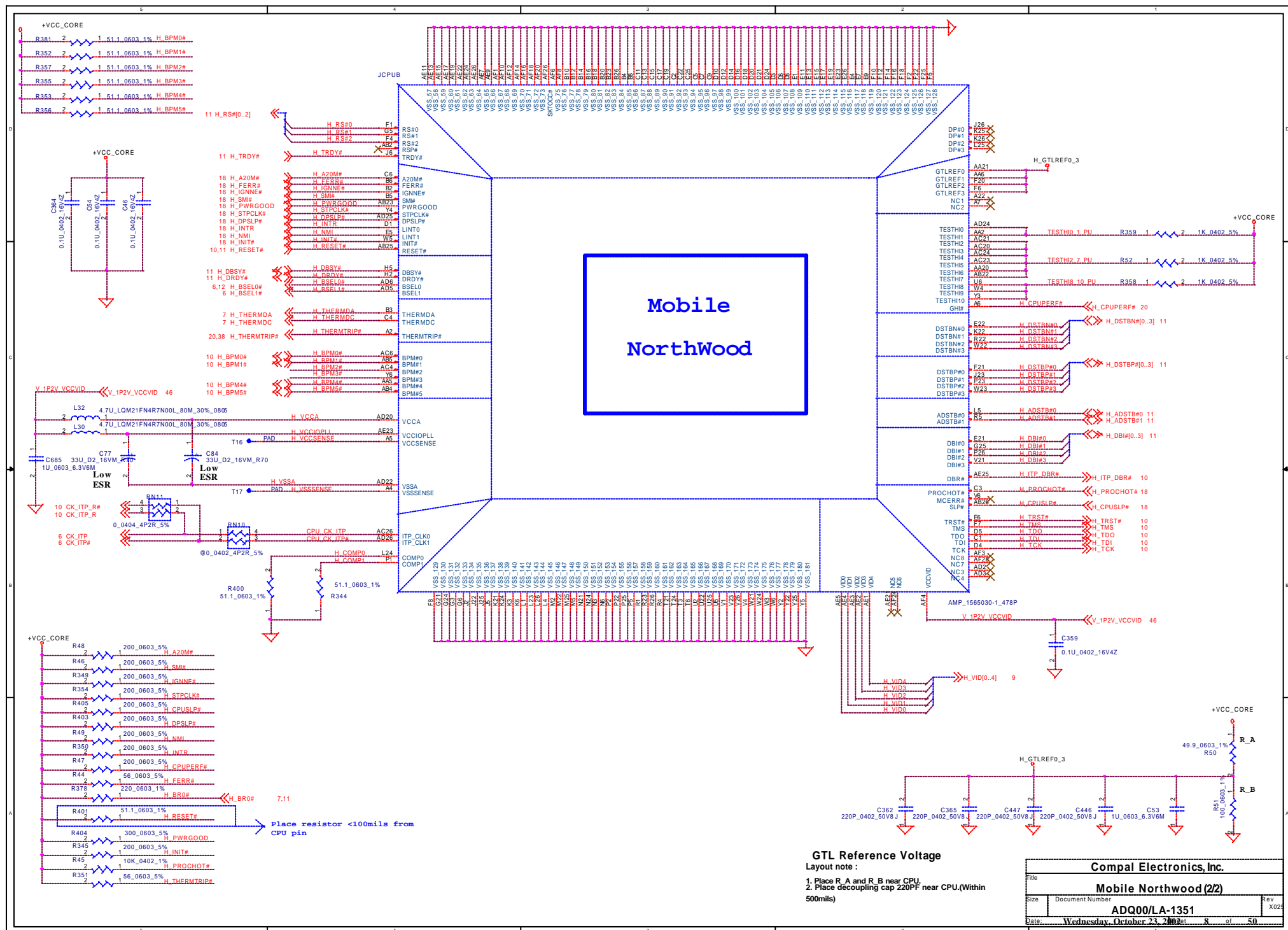




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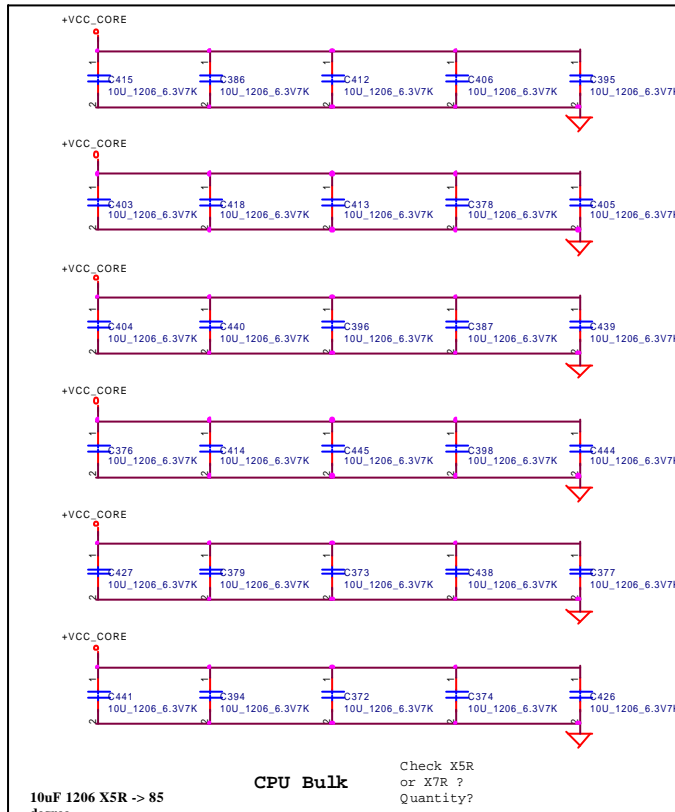






**Layout note :**

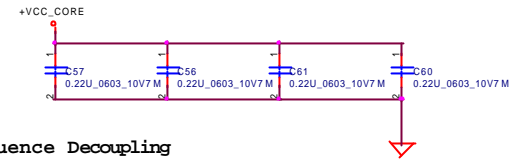
Place close to CPU. Use 2-3 vias per PAD.  
Place 22uF caps underneath balls on solder side.  
Place 10uF caps on the peripheral near balls.  
Use 2-3 vias per PAD.



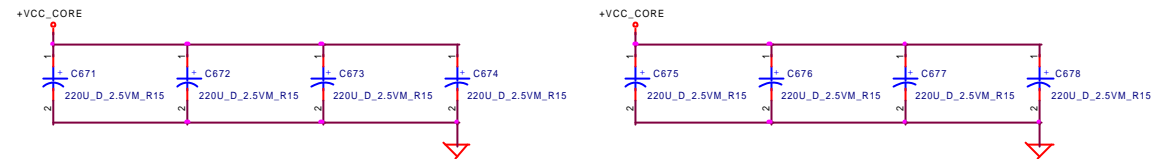
V I D					Vcore
VID4	VID3	VID2	VID1	VID0	V
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950

**Layout note :**

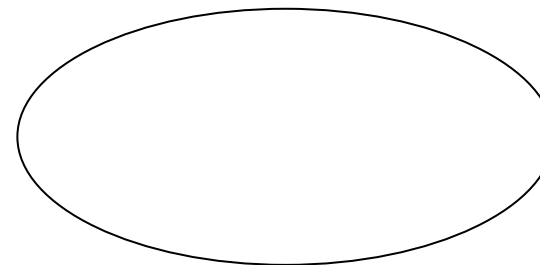
Place close to CPU power and ground pin as possible (<1inch)



To find 2V BULK CAP.

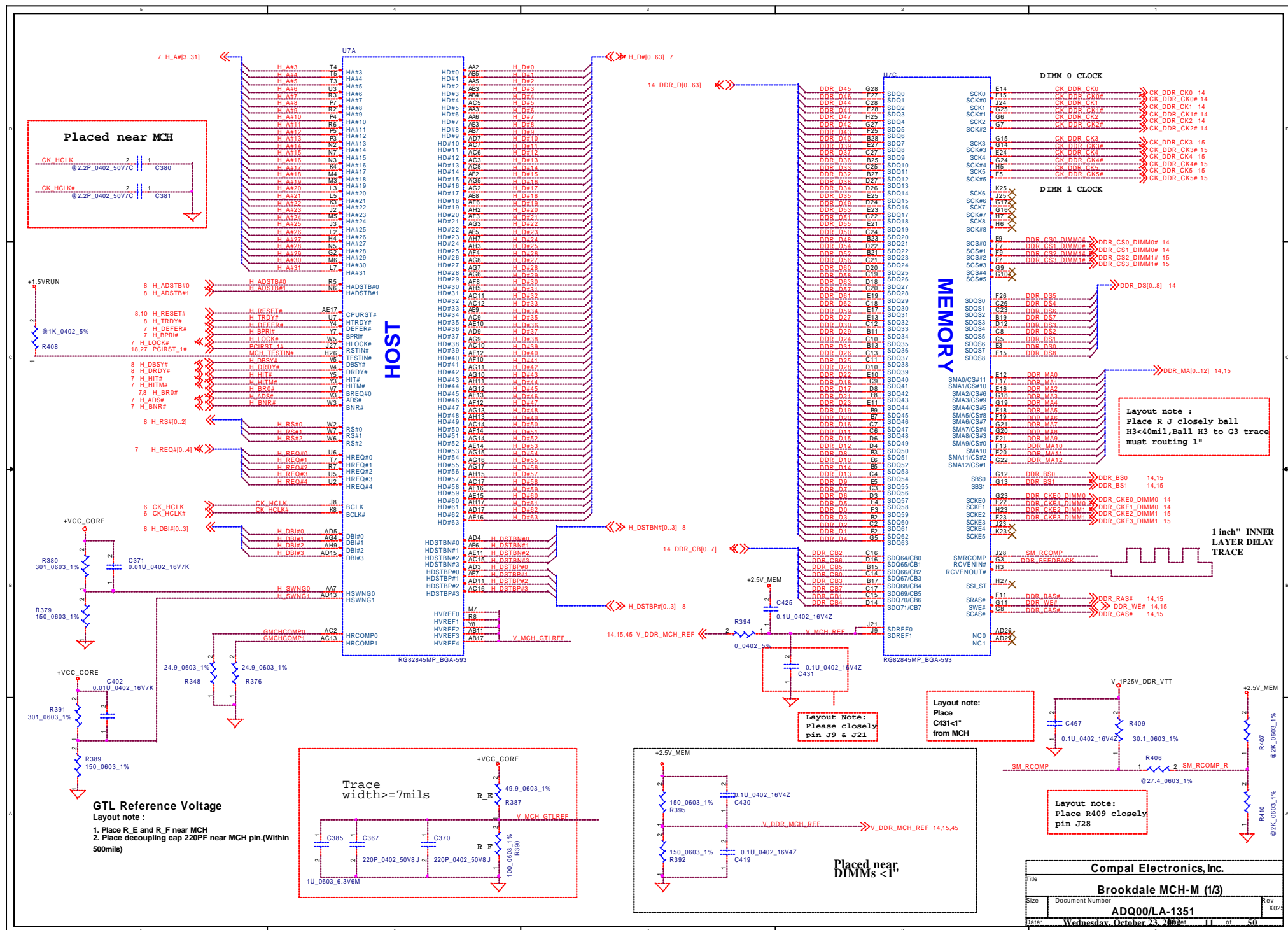


8 H\_VID[0..4]



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CPU bypass and CPU VID		
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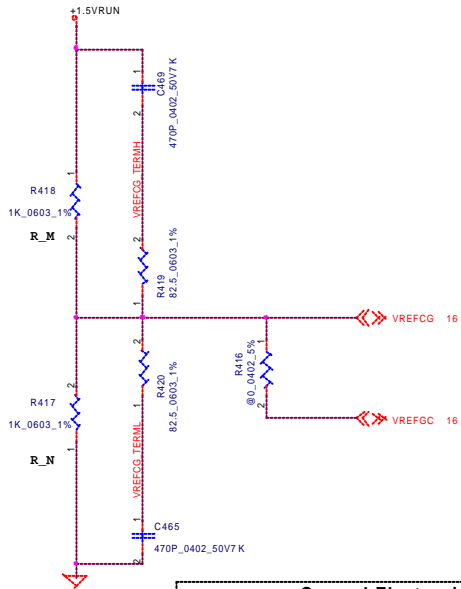
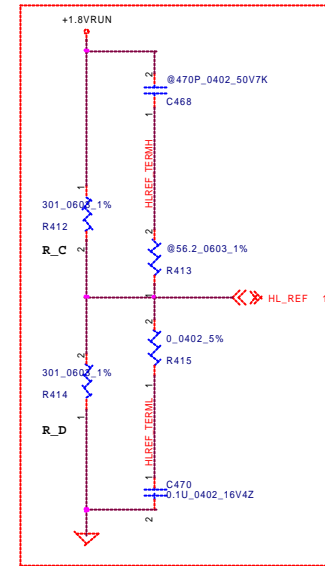




## HUB Interface Reference

Layout note :

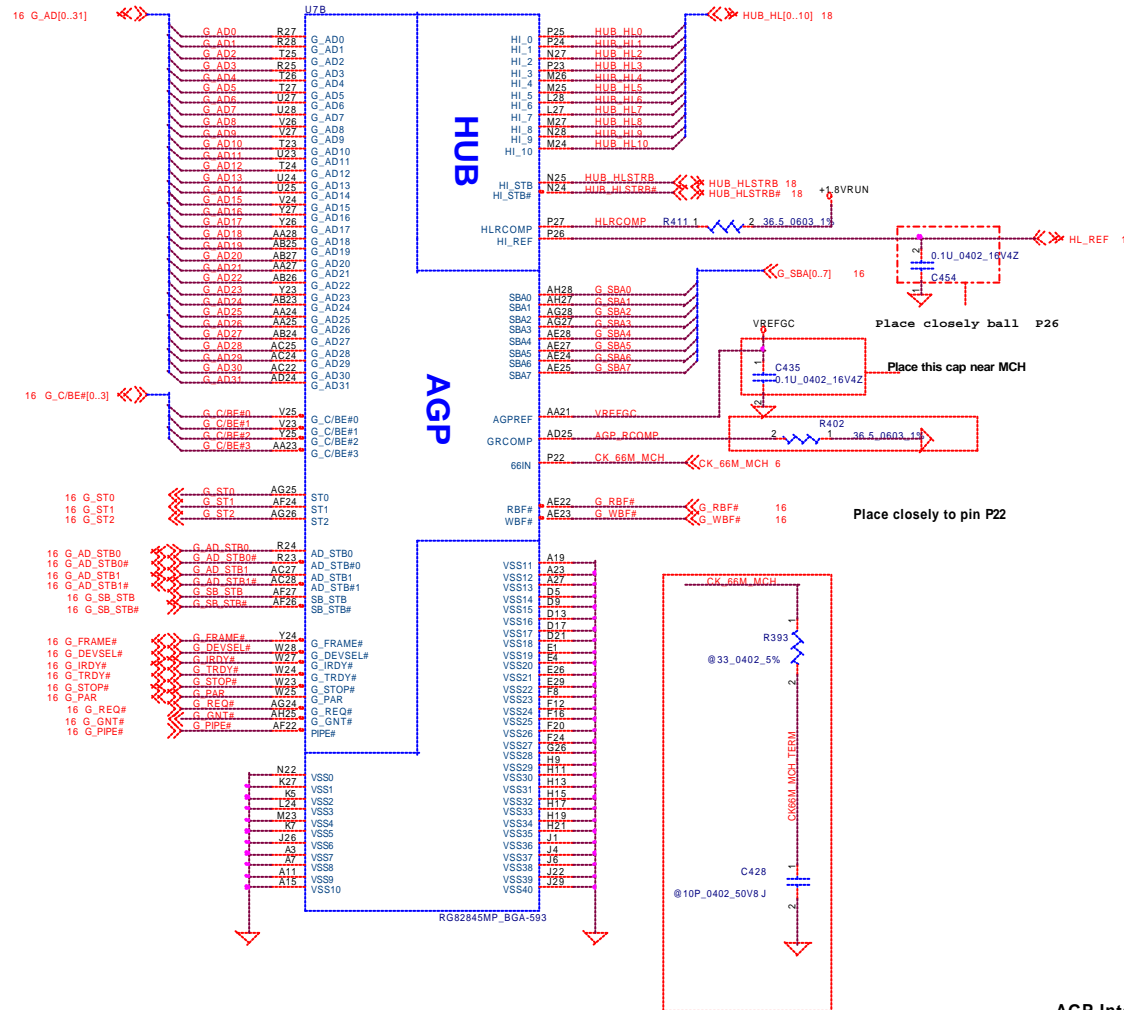
1. Place R\_C and R\_D in middle of Bus.
2. Place capacitors near MCH.



## AGP Interface Reference

Place close to MCH-M

Compal Electronics, Inc.		
Brookdale MCH-M (2/3)		
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G\_ST0  
0=System memory is DDR  
1=System memory is SDR

G\_ST1  
0=533Mhz  
1=400Mhz





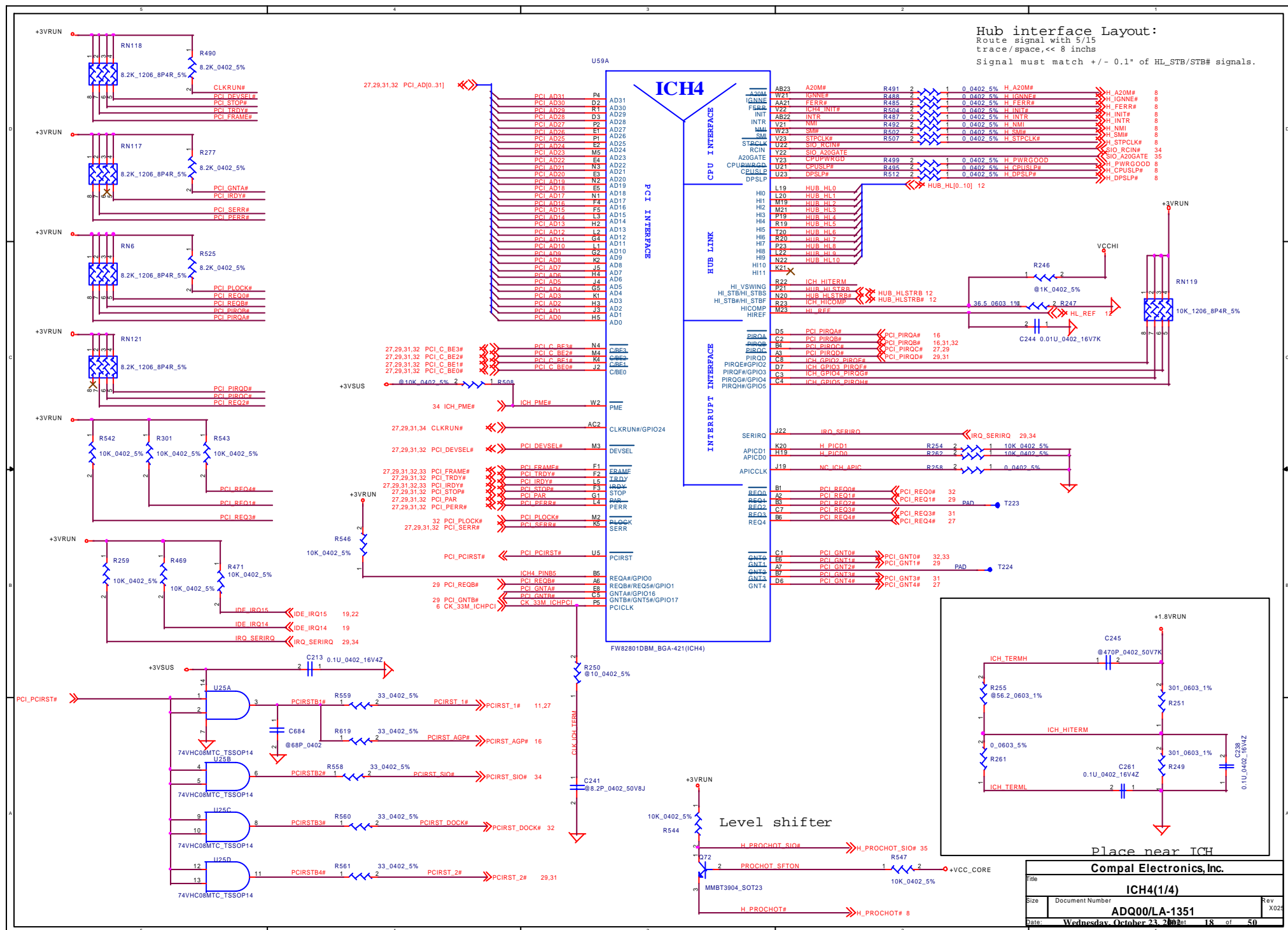




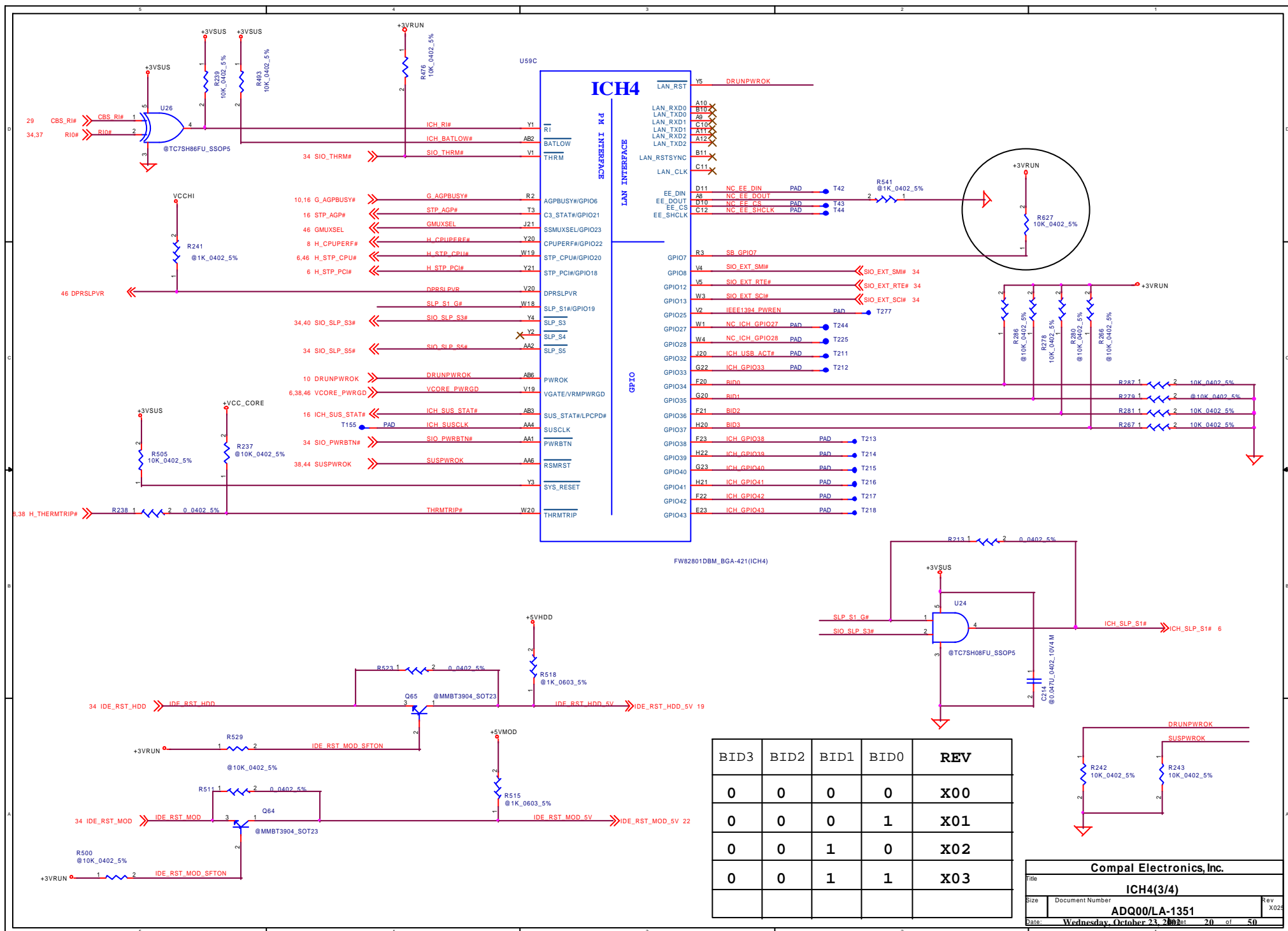




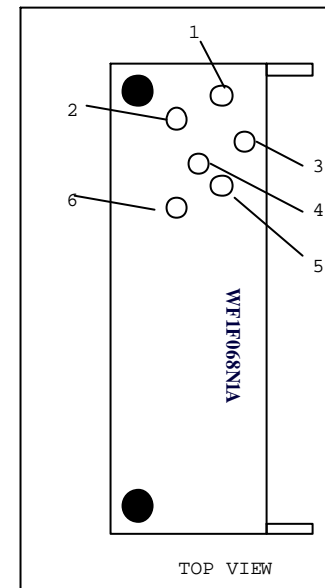
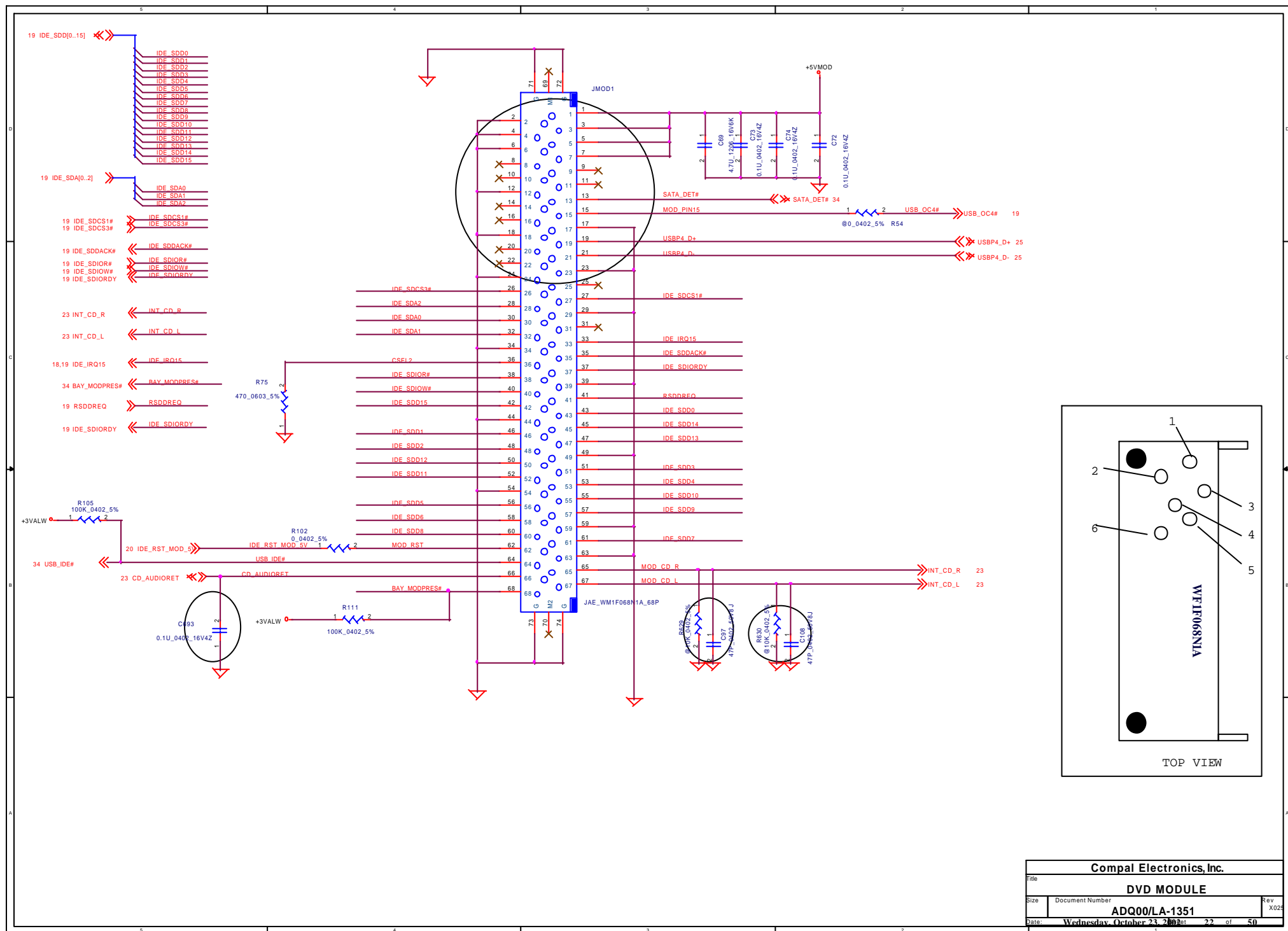












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DVD MODULE		
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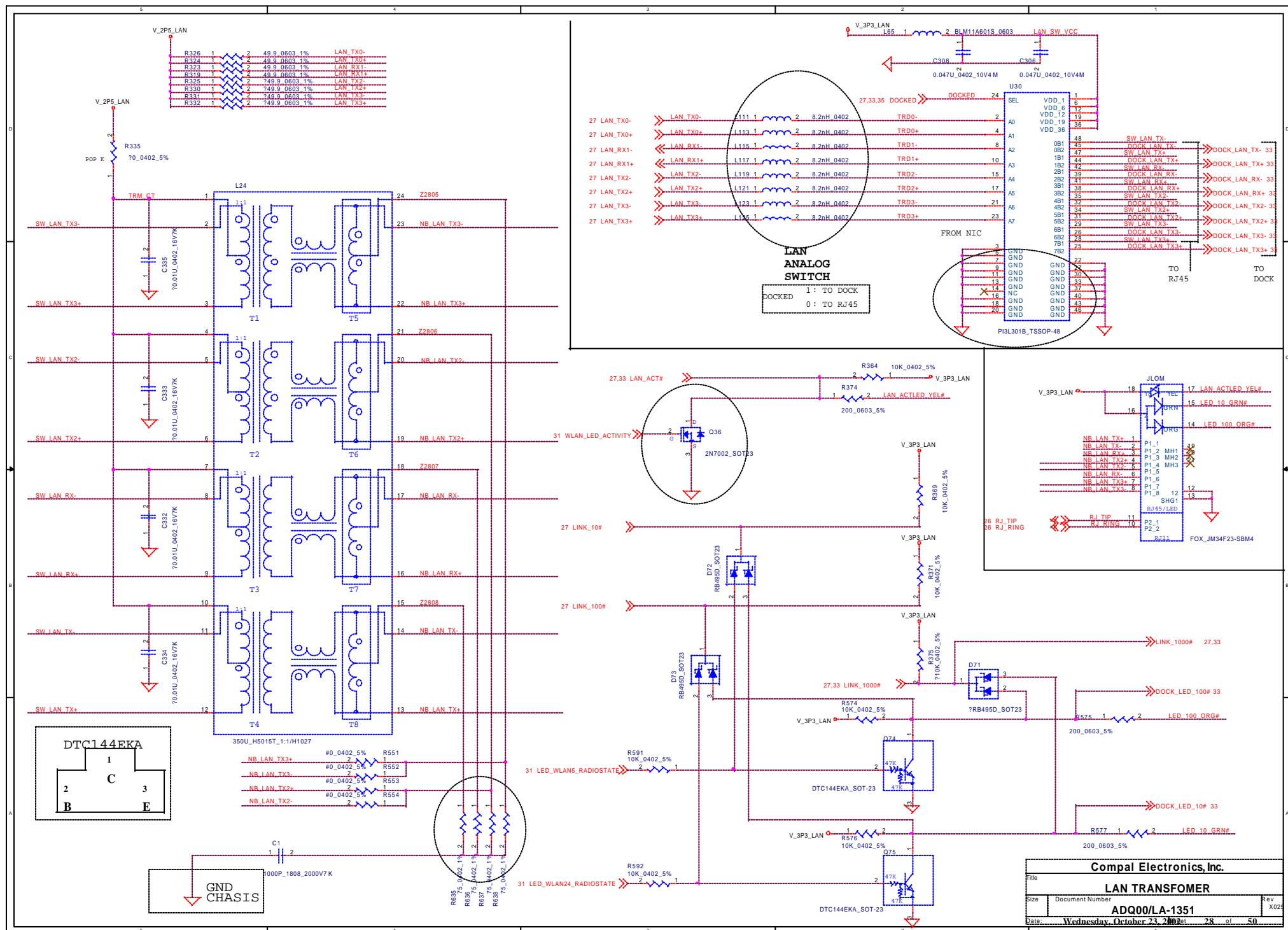


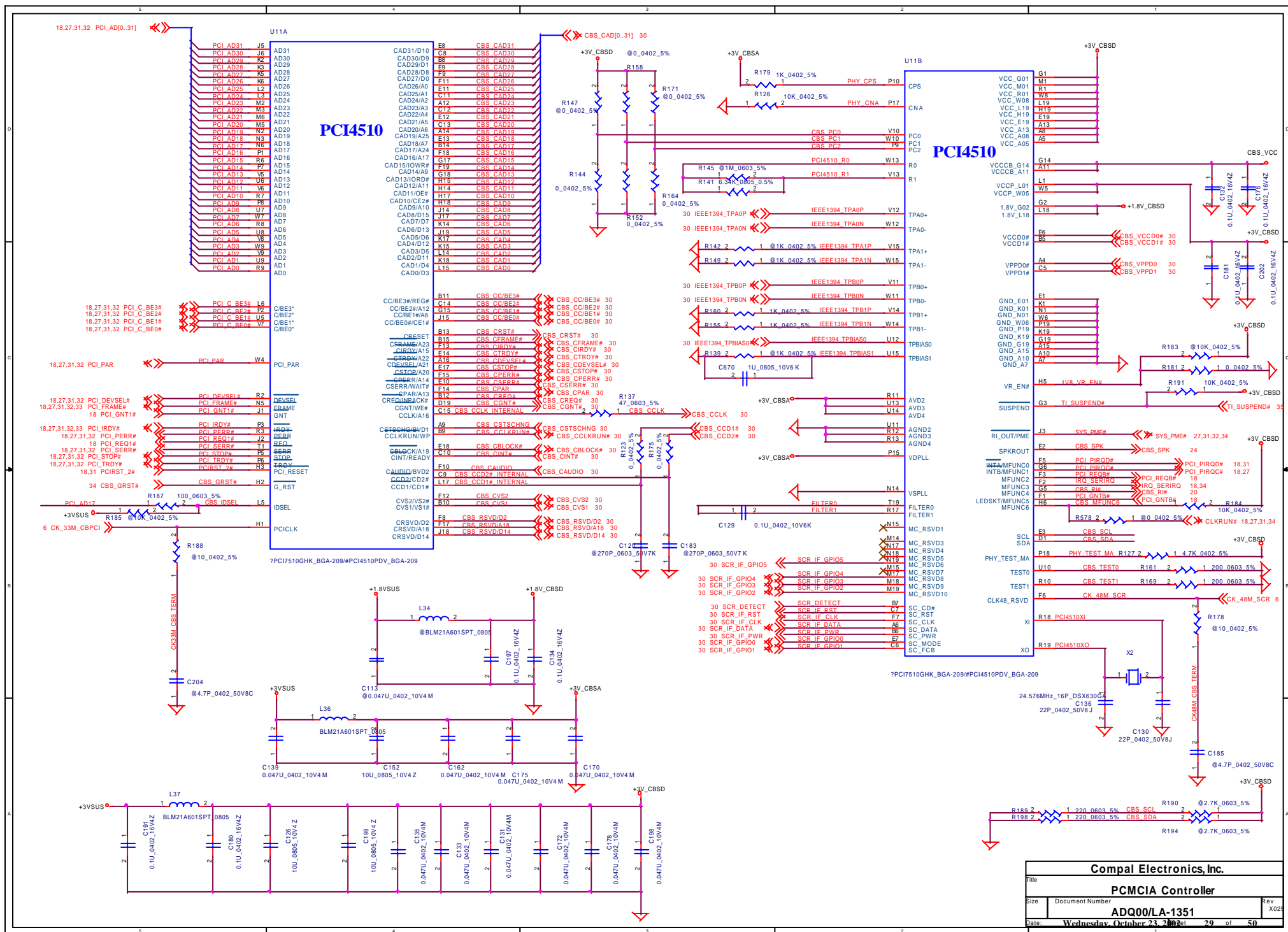


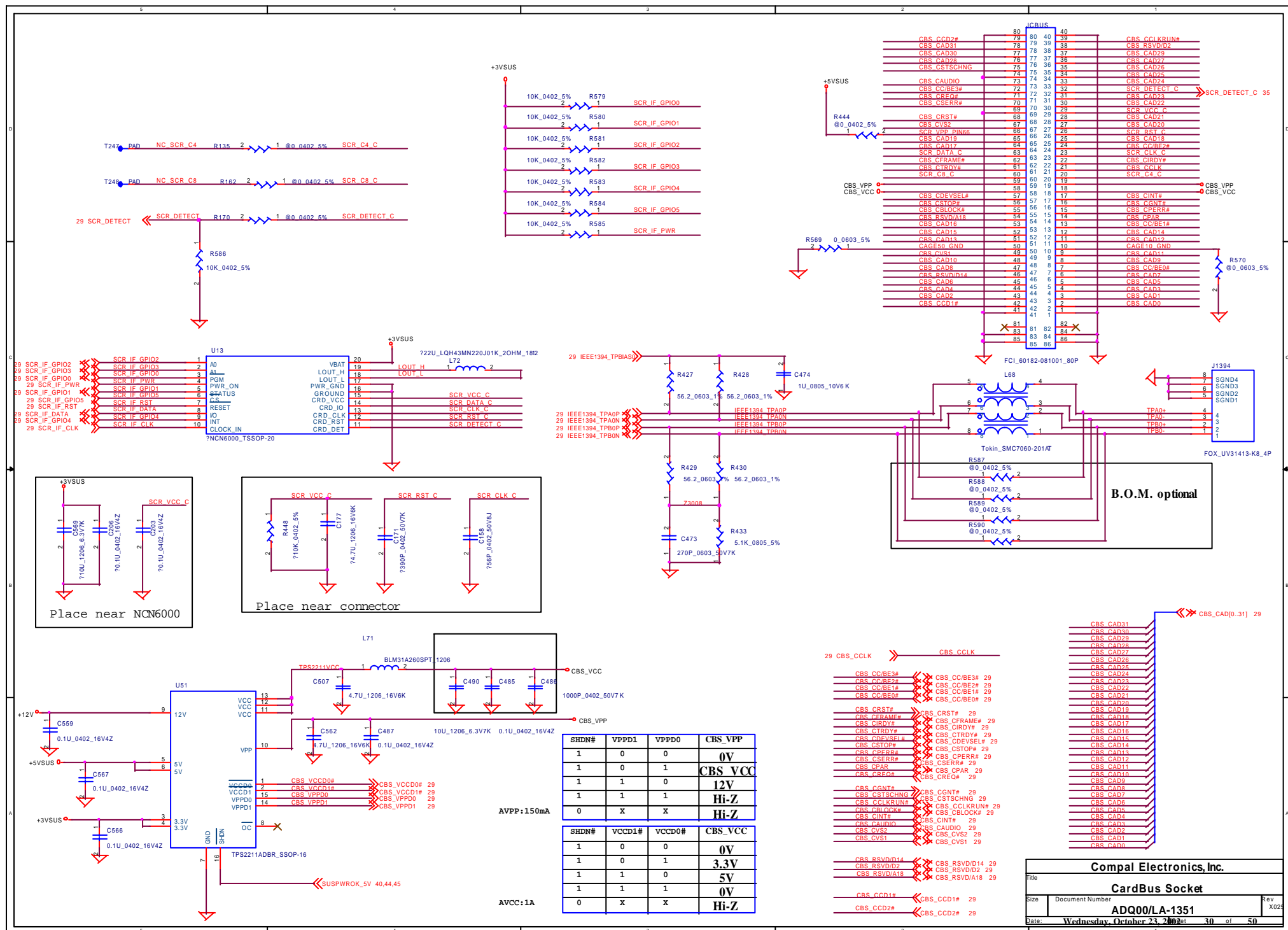






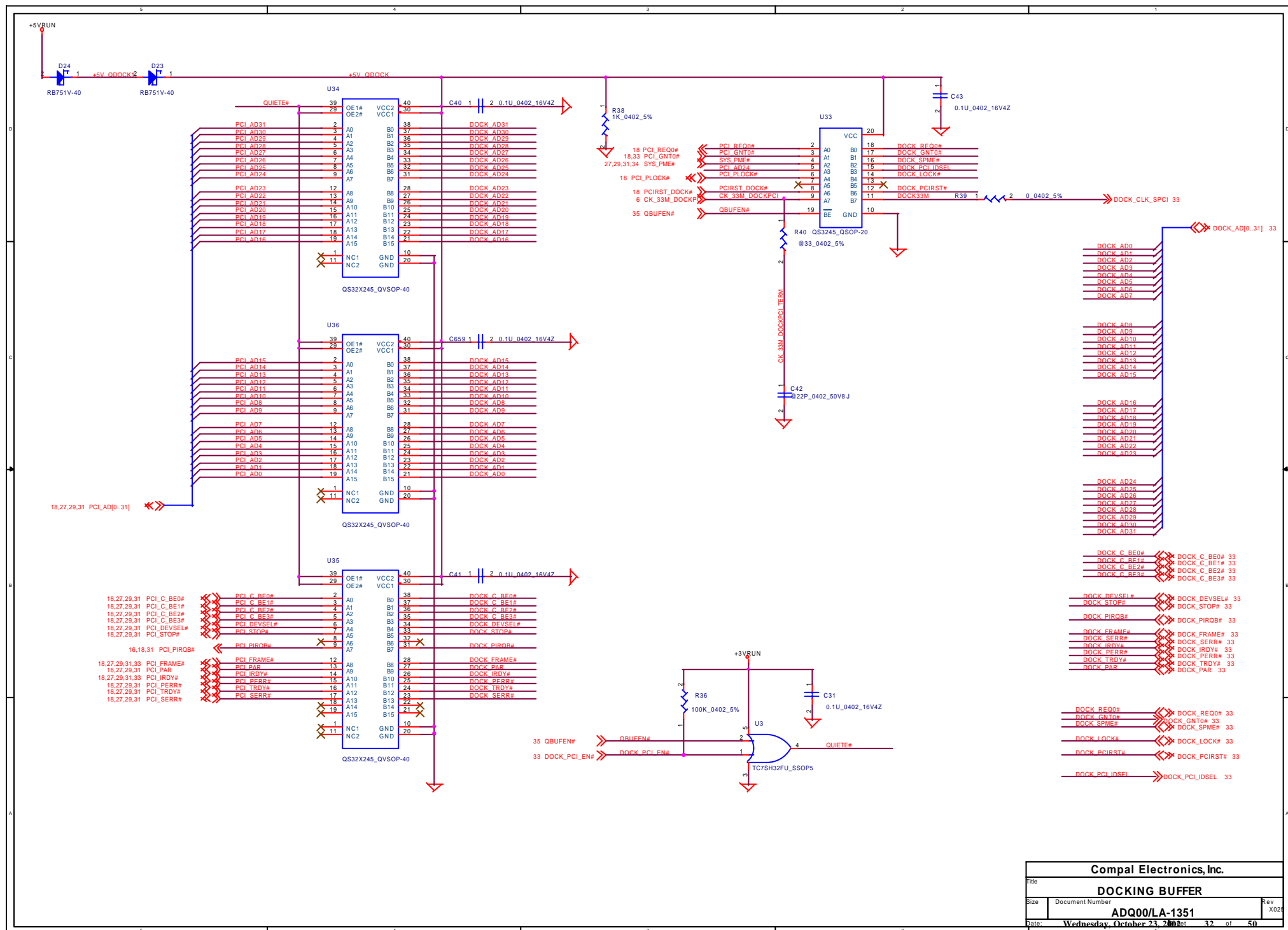




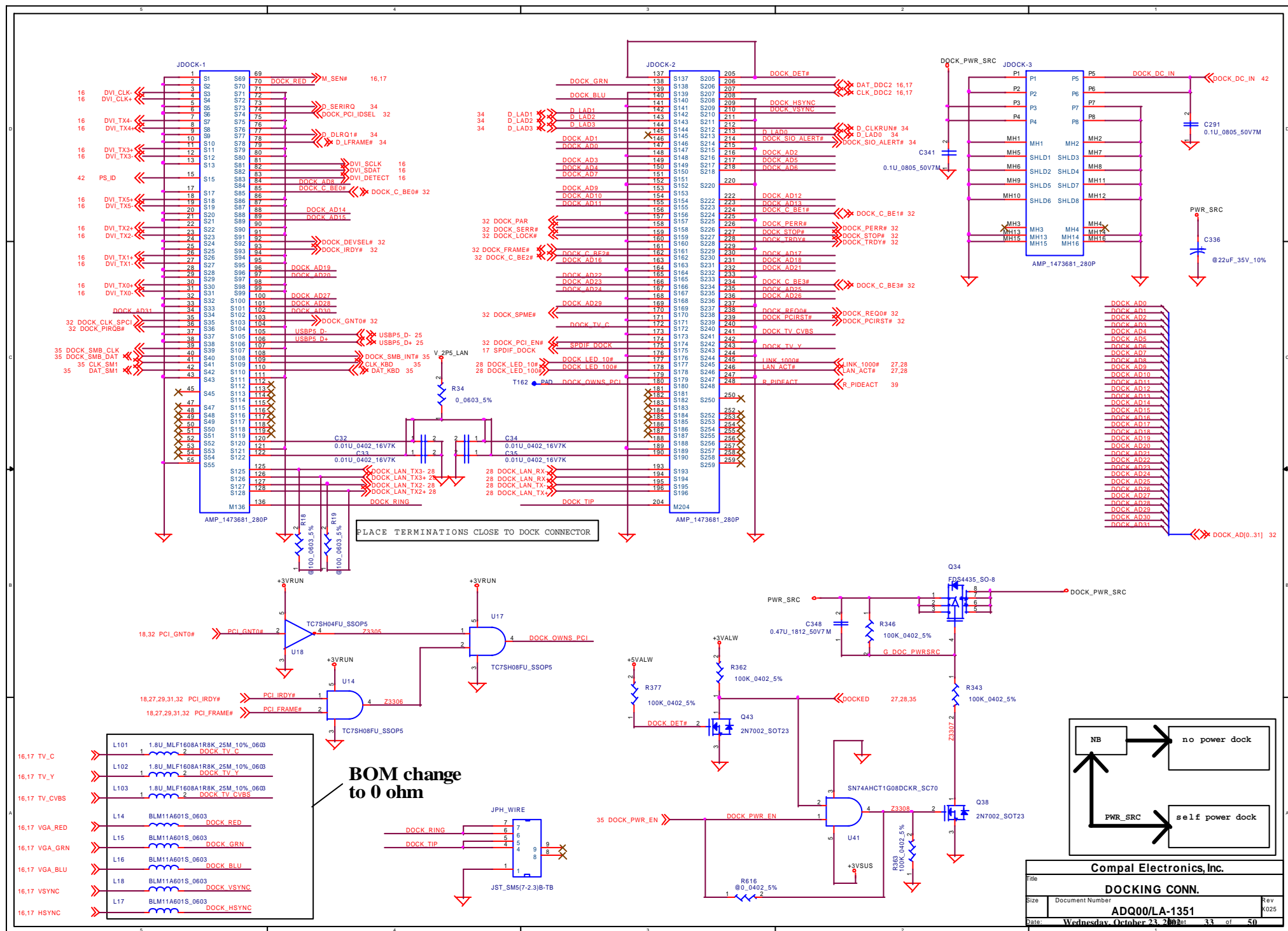








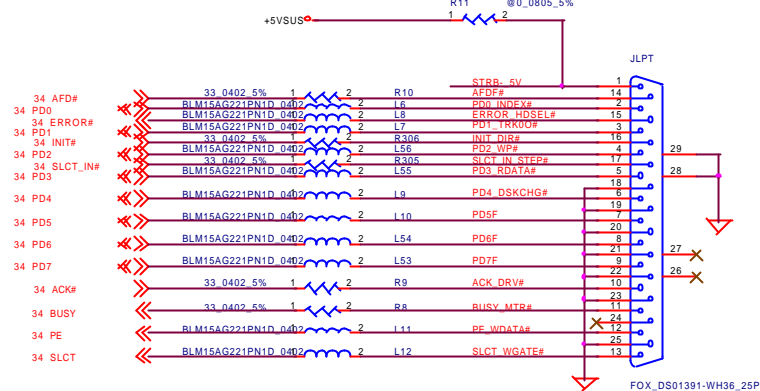
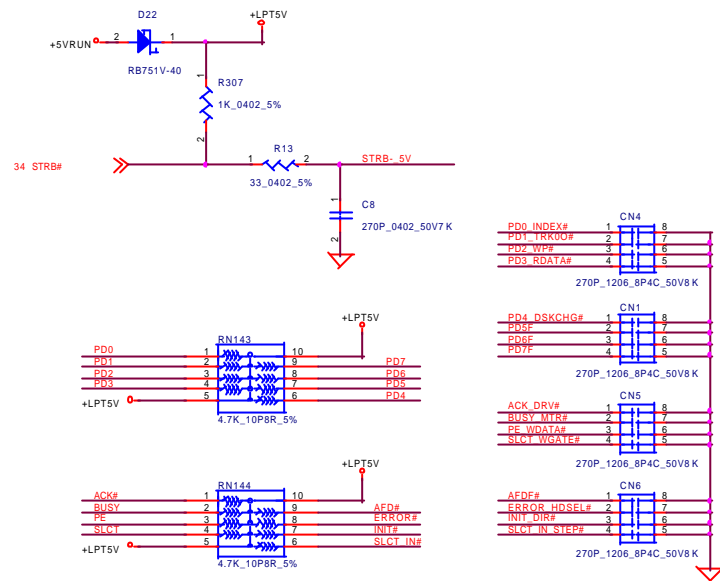




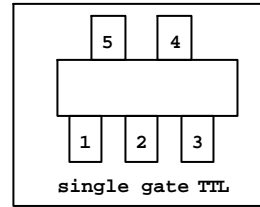
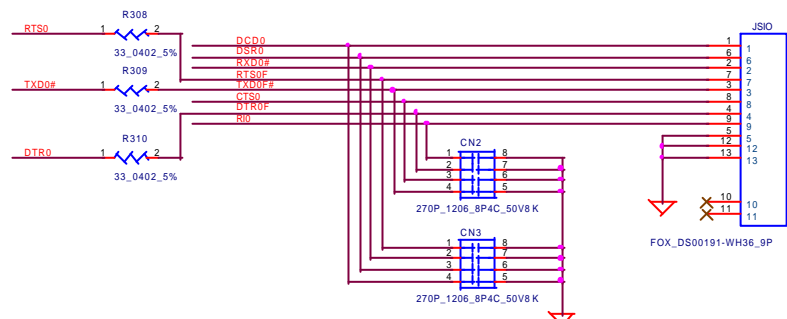
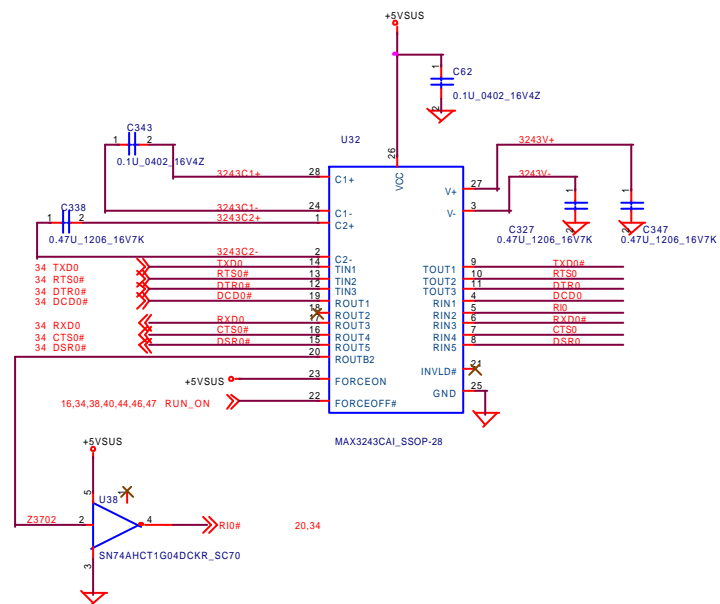








Parallel Port



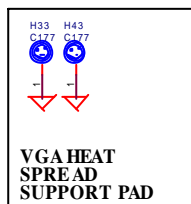
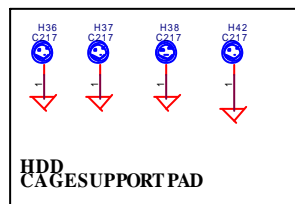
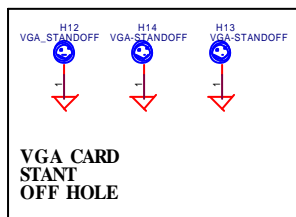
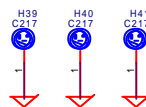
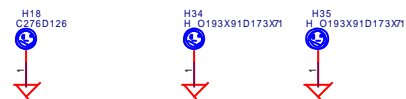
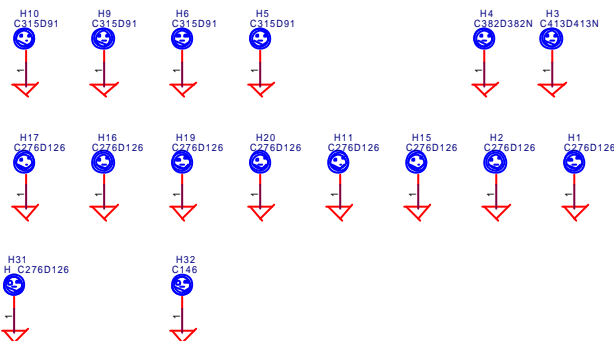
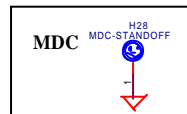
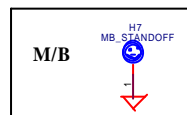
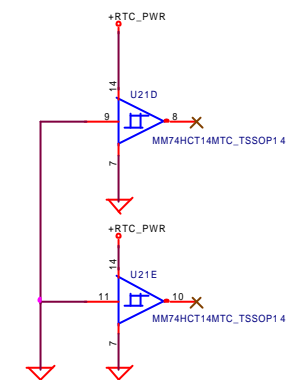
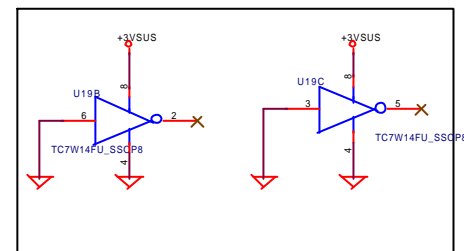
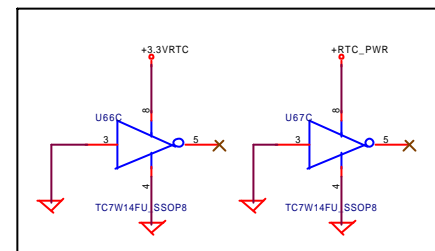
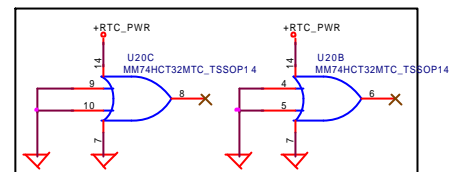
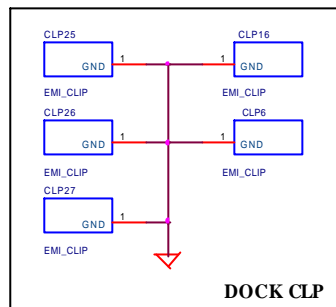
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LPT/SIO/RTC		
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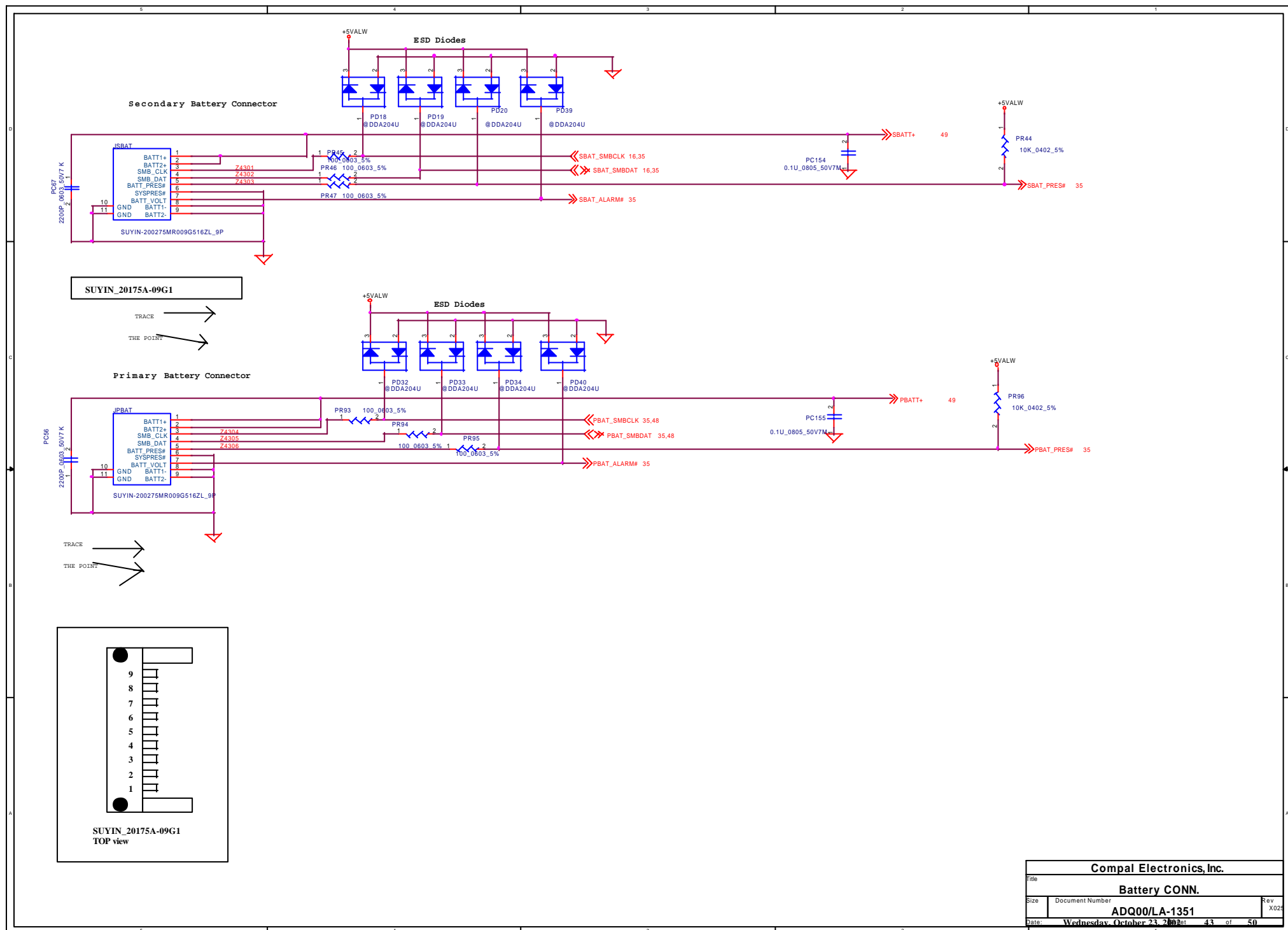


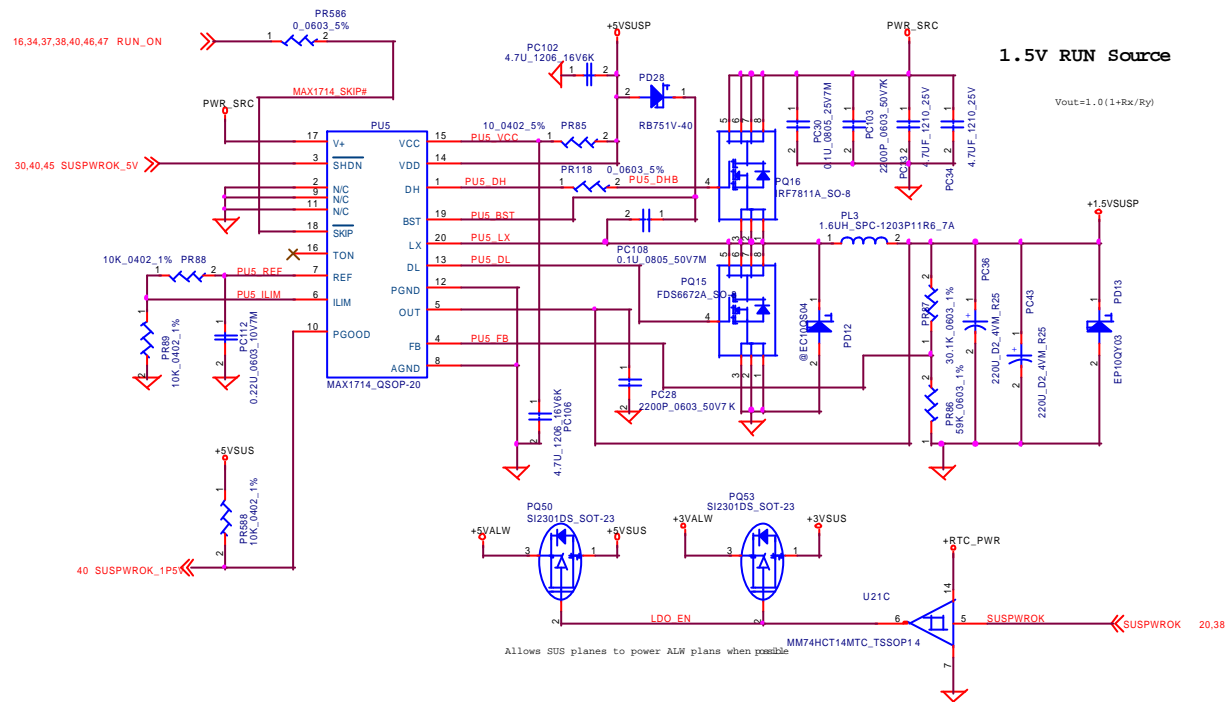




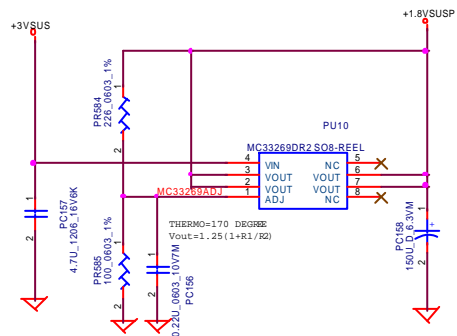






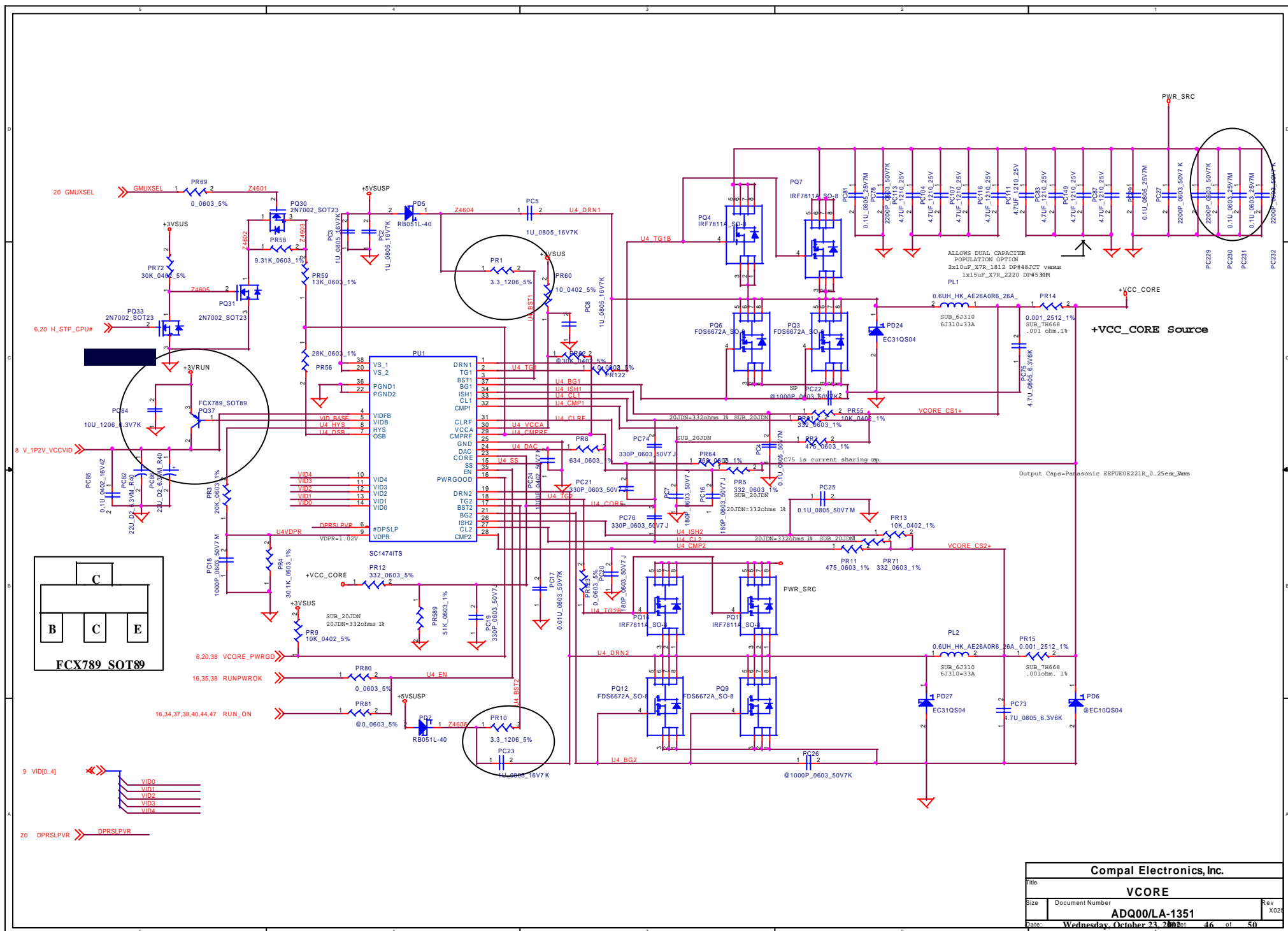


### +1.8V SUS Source

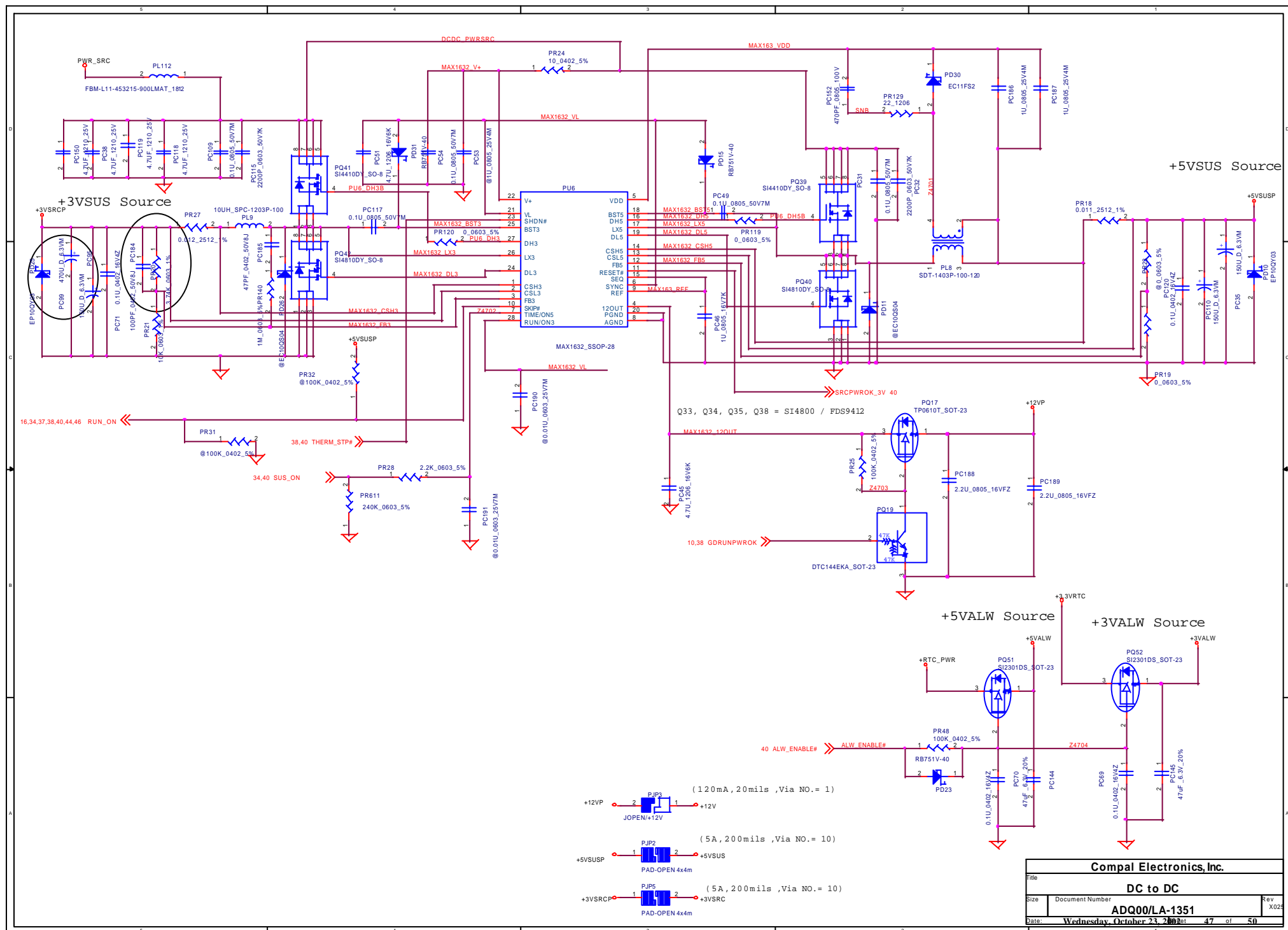


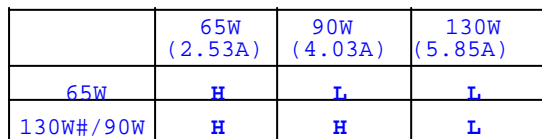
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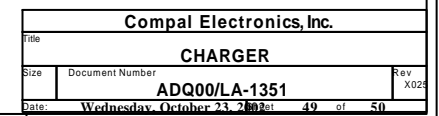


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VCORE			
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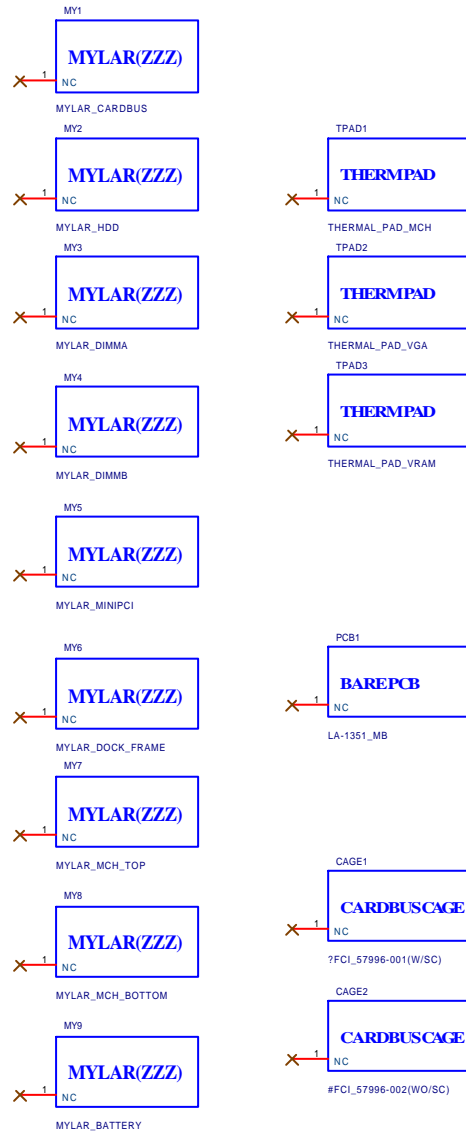






THIS PAGE IS ONLY FOR  
B.O.M. INFORMATION

**PIR**



ITEM	PAGE	REV.	NOTE		
1	9	X025	remove CPU VCCID jumper		
2	19	X025	Change R537 to 1K for PIDEACT# PU		
3	20	X025	remove SIO_LID_EC# signal, PU ICH4GPIO to +3VRUN		
4	21	X025	change JMOD1 pin8,10,14,16,9,11, to NC,conect SATA_DET# to pin13	reserve C693,R629,R630 for CD AUDIO termination	
5	25	X025	change Q1,F1,F2,L25 part to meet Doghouse power current requirement	add R639 for USB port 3 power enable, reserve R640	
6	27	X025	add L109, L110 for BCM4401 PCI power for WOL issue		
7	28	X025	add eight 8.2uH inductor to TX/RX line	seperate RN1 to 4 small resistors	Change Q36 to 2N7002
8	29	X025	remove D11 for TI_SUSPEND#		
9	31	X025	Change JPC11 pin109 and pin 123 to NC and remove R457,C576		
10	34	X025	add R628 PU to U27 pin D12		
11	35	X025	reserve R634 for TI_SUSPEND#		
12	38	X025	change OTP to discrete solution		
13	40	X025	change Q12 and Q77 to SI4810		
14	42	X025	remove AC LOW PRES circuit		
15	46	X025	change PQ37 to FCX789	remove PC147 change PR1,PR10 to 3.3ohm	add PC229,PC230,PC231,PC232
16	47	X025	change PR20 to 3.74K		
17	48	X025	addPC228,change C202,PC203, PC204,PC211,PC212,PC213,PC214 to 10uF/25V	Change PL120 to 6uH	

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